AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A plugging method for a printed circuit board having a plurality of ~~first~~ circuit patterns formed on a surface of the board~~, a plurality of second circuit patterns formed in the board~~, comprising the steps of:

filling a solder resist or resin in ~~spaces~~ a space between ~~the first~~ two adjacent circuit patterns by moving a squeegee to be abutted directly on an upper surface of at least one of the two adjacent circuit patterns~~;~~

~~grinding the surface of the board; and~~

~~performing a two dimensional plating on an upper surface of the first pattern~~.

2. (Currently Amended) The method of claim ~~1~~17, wherein the two dimensional plating is a gold plating.

3. (Currently Amended) A method for manufacturing a printed circuit board having a plurality of first circuit patterns formed on a surface of the board and a plurality of second circuit patterns formed within the board, and a plurality of via holes for electrically connecting the first circuit patterns and the corresponding second circuit patterns, comprising the steps of:

filling a solder resist or resin in ~~spaces~~ at least one of the via holes~~between the circuit patterns formed on the surface of the board~~ by moving a squeegee to be abutted directly on an upper surface of at least one of the first circuit patterns corresponding to the at least one of the via holes;

~~grinding the surface of the board and exposing an upper surface of the circuit patterns formed on the surface of the board; and~~

~~performing a two dimensional plating on the exposed upper surface of the circuit pattern formed on the surface of the board.~~

4. (Currently Amended) The method of claim ~~3~~18, wherein the two dimensional plating is a gold plating.

5. (Currently Amended) A plugging method for a printed circuit board having a plurality of first circuit patterns formed on a surface of the board, and a plurality of second circuit patterns formed in the board, comprising the steps of:

filling a solder resist or resin in spaces between the first circuit patterns;

grinding the surface of the board; and

performing a two dimensional plating on an upper surface of the first pattern;~~The method of claim 1,~~

wherein the solder resist or ~~insulating~~ resin is plugged into the ~~hole~~ spaces by moving the squeegee under the condition of being abutted directly on the upper surface of the ~~hole~~spaces.

6. (Currently Amended) The method of claim 1, wherein the step of filling the solder resister or resin comprises;

a first step of plugging the solder resist or ~~insulating~~ resin in one portion of the ~~hole~~ space by moving the squeegee ~~under the condition of being~~to be abutted on the upper surface of the at least one of the two adjacent circuit patterns~~hole~~; and

a second step of completely plugging the solder resist or ~~insulating~~ resin in the whole portion of the ~~hole~~ space by moving the squeegee ~~under the condition of being~~to be abutted on the upper surface of the at least one of the two adjacent circuit patterns~~hole~~.

7. (Currently Amended) The method of claim 6, wherein in the second plugging step the solder resist or ~~insulating~~ resin is plugged in the ~~hole~~ space by moving the squeegee in ~~the~~ an opposite direction to ~~the~~ a moving direction of the squeegee in the first plugging step.

8. (Currently Amended) The method of claim 6, wherein in the second plugging step the solder resist or ~~insulating~~ resin is plugged in the ~~hole~~ space by moving the squeegee in ~~the~~ a same direction to ~~the~~ a moving direction of the squeegee in the first plugging step.

9. (Currently Amended) The method of claim 1, wherein the solder resist or ~~insulating~~ resin is coated only on an area exposed by a mask for selectively exposing the plurality of circuit patterns formed on the printed circuit board at a predetermined interval or on the ~~hole~~space.

10. (Currently Amended) ~~The method of claim 1,~~ A plugging method for a printed circuit board having a plurality of first circuit patterns formed on a surface of the board, and a plurality of second circuit patterns formed in the board, comprising the steps of:

filling a solder resist or resin in spaces between the first circuit patterns;

grinding the surface of the board; and

performing a two dimensional plating on an upper surface of the first pattern;

wherein the solder resist or ~~insulating~~ resin filled in the spaces among the surface side circuit patterns is filled to the same height as the upper surface of the circuit patterns.

11. (Currently Amended) The method of claim 3, wherein the solder resist or ~~insulating~~ resin is plugged into the at least one of the via holes by moving the squeegee ~~under the condition of being~~to be abutted directly on ~~the~~ an upper surface of the at least one of the via holes.

12. (Currently Amended) The method of claim 3, wherein the step of filling the solder resister or resin comprises~~;~~:

a first step of plugging the solder resist or ~~insulating~~ resin in one portion of the at least one of the via holes by moving the squeegee ~~under the condition of being~~to be abutted on the upper surface of the at least one of the first circuit patterns~~hole~~; and

a second step of completely plugging the solder resist or ~~insulating~~ resin in the whole portion of the at least one of the via holes by moving the squeegee under the condition of being abutted on the upper surface of the at least one of the first circuit patterns~~hole~~.

13. (Currently Amended) The method of claim 12, wherein in the second plugging step the solder resist or ~~insulating~~ resin is plugged in the at least one of the via holes by moving the squeegee in ~~the~~ an opposite direction to ~~the~~ a moving direction of the squeegee in the first plugging step.

14. (Currently Amended) The method of claim 12, wherein in the second plugging step the solder resist or ~~insulating~~ resin is plugged in the at least one of the via holes by moving the squeegee in ~~the~~ a same direction to ~~the~~ a moving direction of the squeegee in the first plugging step.

15. (Currently Amended) The method of claim 3, wherein the solder resist or ~~insulating~~ resin is coated only on an area exposed by a mask for selectively exposing the plurality of the first circuit patterns formed on the printed circuit board at a predetermined interval or on the via holes.

16. (Currently Amended) The method of claim 3, wherein the solder resist or ~~insulating~~ resin filled in the ~~spaces~~ at least one of the via holes ~~among the surface side circuit patterns~~ is filled to the same height as the upper surface of the first circuit patterns.

17. (New) The method of claim 1, further comprising:

grinding the surface of the board; and

performing a two dimensional plating on an upper surface of at least one of the circuit patterns.

18. (New) The method of claim 3, further comprising:

grinding the surface of the board and exposing an upper surface of at least one of the first circuit patterns formed on the surface of the board; and

performing a two dimensional plating on the exposed upper surface of the at least one of the first circuit patterns formed on the surface of the board.